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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,542	01/05/2001	Randal N. Linden	1005/204	5270

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EXAMINER	
RAMPURIA, SATISH	
ART UNIT	**PAPER NUMBER**
2124	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/755,542	LINDEN, RANDAL N.	
	Examiner	Art Unit	
	Satish S. Rampuria	2124	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004 (RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed on November 1, 2004.

2. Claims 5-39 are pending.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on Nov 1, 2004 has been entered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 5-8, 10, 11, 16, 17, 19-25, 30, 32, 35, and 37-39 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,031,992 to Cmelik et al., hereinafter called Cmelik.

Per claim 5:

Cmelik discloses:

- A method of generating target instructions from a plurality of first instructions, the target instructions executable on a target processor (col. 4, lines 41-44 "the target application is run on the host processor... a partial target operating system... which the target application generates"), comprising:
- analyzing the plurality of first instructions (col. 9, lines 24-25 "a target instructions set"), en mass by an information processing system to break down the functional operations encoded by the first instructions (col. 9, lines 31-50 "instructions set translated... with speculations" and col. 16 and 17, 57-67 and 1-30 "a translated instruction... target instruction was addressed");
- generating the target instructions by an information processing system based on the information representing the information flow (col. 9, lines 29-30 "to translate a set of target instructions into instructions of a host instruction set"), in preference over particular operations specified by individual ones of the plurality of first instructions (col. 9, lines 33-40 "instructions set translated... by microprocessor").

Per claim 6:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein the first instructions are not executable on the target processor (col. 3, lines 43-47 "The emulator software changes the target instructions of an application program

written for the target processor family into host instructions capable of execution by the host microprocessor").

Per claim 7:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein the information representing the information flow is produced and the target instructions are generated at run-time, after accessing the plurality of first instructions from a predetermined memory (col. 9, lines 23-26 "a host computer designed to execute target programs for a target computer having a target instruction set comprising the combination of software"), the method further comprising executing the target instructions without requiring the target instructions to be first stored to the predetermined memory (col. 12, lines 15-16 "host translates instructions into instructions for the morph host on the fly").

Per claim 8:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein individual ones of the target instructions are generated without regard to particular operations specified by the individual ones of the plurality of first instructions (col. 9, lines 47-49 "to translate a new set of host instructions without the speculation when a set of host instructions fails to execute in accordance with the speculation").

Per claim 10:

The rejection of claims 5 and 12 are incorporated, respectively and further, Cmelik discloses:

- wherein the target instructions are generated in a manner to reduce a number of machine cycles required to execute the target instructions (col. 3, lines 51-57 "the host computers executing target programs using emulation software utilize reduced instruction set (RISC) microprocessors because RISC processors are theoretically simpler and consequently can run faster than other types of processors").

Per claims 11 and 23:

The rejection of claim 5 is incorporated, respectively, and further, Cmelik discloses:

- wherein the number of machine cycles is reduced in relation to the number of machine cycles that would be required to execute instructions according to a literal translation of the plurality of first instructions into the second machine language (col. 7, lines 63-65 "the host operating system is already designed to respond to the same calls that the target application generates so that the generation of virtual devices is considerably reduced". Also, fig. 1(d) and related description.).

Per claim 21:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein the step of generating the target instructions includes translating first operations specified by the plurality of first instructions to target operations different from the first operations (col. 9, lines 29-30 "to translate a set of target instructions into instructions of a host instruction set") to reduce the number of machine cycles required to executed the

target instructions (col. 27, lines 52-65 "the length of the target instruction is added to the value in the working instruction pointer register (Reip)... a commit instruction is executed... the commit instruction copies the current value of each working register which is shadowed into its associated official target register and moves a pointer value designating the position of the gate of the gated store buffer from immediately in front of the uncommitted stores to immediately behind those stores so that they will be placed in memory").

Per claims 16 and 17:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein at least one of the target instructions is generated to specify a second physical operation that is different from, but equivalent to a first physical operation specified by one or more instructions of the plurality of first instructions (col. 8, lines 38-41 "maps the operations of the computer for which the application was designed to the hardware resources of the host machine in order to carry out the operations of the program being run").

Per claims 19, 20, and 22:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein the step of generating the target instructions includes eliminating operations specified by the plurality of first instructions which are unnecessary to achieve the determined purpose (col. 9, lines 34-39 "to optimize the instructions of the host

instruction set translated from the target program speculating upon the occurrence of a condition, means to determine under control of the software official state of the target computer which existed at the beginning of a translation of a set of target instructions during execution of the target program by the microprocessor").

Claims 24-25, and 30 are the computer program product claim corresponding to method claims 5, 7, and 19 respectively, and rejected under the same rational set forth in connection with the rejection of claims 5, 7, and 19 respectively, above.

Claims 32, 35, 37, and 38 are the system claim corresponding to method claims 5, 11, 19, and 12 respectively, and rejected under the same rational set forth in connection with the rejection of claims 5, 11, 19 and 12 respectively, above.

Claim 39 is the system claim corresponding to method claims 5, 6, 14, 15, and 16 respectively, and rejected under the same rational set forth in connection with the rejection of claims 5, 6, 14, 15, and 16 respectively, above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9, 12-15, 18, 26-29, 31, 33, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cmelik in view of admitted prior art.

Per claim 9:

The rejection of claim 5 is incorporated, and further, Cmelik does not explicitly disclose wherein the plurality of first instructions are according to a first machine language and of a type executable by a first processor but not the target processor, and the target instructions are according to a second machine language and of a type executable by the target processor.

However, admitted prior art discloses wherein the plurality of first instructions are according to a first machine language and of a type executable by a first processor but not the target processor, and the target instructions are according to a second machine language and of a type executable by the target processor (Applicant's specification, page 3, lines 3-9 "a target, will include an emulator that allows the target computer to emulate the instructions, called the source, of another type of CPU. Thus, the target computer will have stored in memory source instructions that may be called in response to applications software, target instructions emulating the source instructions and executable by the target CPU, and an emulator that causes one or more target instructions to be executed in response to a given source instruction. Thus, the given computer can execute target").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of having the independent instructions executing on host and target processor as taught in admitted prior art into the method of automatic analyzing and generating the instructions for the target processor as taught by Cmelik. The modification would be obvious because of one of ordinary skill in the art would be

motivated to have the independent instructions executing on the host and target processor to provide the less use of memory by the processors as suggested in admitted prior art (pages 5 and 6, lines 19-23 and 1-6, respectively).

Per claim 12, 18:

The rejection of claim 9 is incorporated, and further, Cmelik discloses:

- wherein the target instructions specify a target number of transfers between a register of the target processor and a memory associated with the target processor, the target number being reduced in relation to a number of transfers specified by the plurality of first instructions between a register of the first processor and memory associated with the first processor (col. 27, lines 52-65 "the length of the target instruction is added to the value in the working instruction pointer register (Reip)... a commit instruction is executed... the commit instruction copies the current value of each working register which is shadowed into its associated official target register and moves a pointer value designating the position of the gate of the gated store buffer from immediately in front of the uncommitted stores to immediately behind those stores so that they will be placed in memory").

Per claim 13, 15:

The rejection of claim 12 is incorporated, respectively, and further, Cmelik discloses:

- wherein the number of transfers is further reduced in relation to the number of transfers resulting from a literal translation of the plurality of first instructions into the second

machine language (col. 7, lines 63-65 "the host operating system is already designed to respond to the same calls that the target application generates so that the generation of virtual devices is considerably reduced". Also, fig. 1(d) and related description.).

Per claim 14:

The rejection of claim 12 is incorporated, respectively and further, Cmelik discloses:

- wherein the target instructions are generated so as to minimize the target number of transfers (col. 3, lines 51-57 "the host computers executing target programs using emulation software utilize reduced instruction set (RISC) microprocessors because RISC processors are theoretically simpler and consequently can run faster than other types of processors").

Claims 26-29 are the computer program product claim corresponding to method claims 9, 12, 13, and 15 respectively, and rejected under the same rational set forth in connection with the rejection of claims 9, 12, 13, and 15 respectively, above.

Claims 31, 33, 34, and 36 are the system claim corresponding to method claims 18, 9, 12, and 15 respectively, and rejected under the same rational set forth in connection with the rejection of claims 18, 9, 12, and 15 respectively, above.

Response to Arguments

8. Applicant's arguments with respect to claims have been considered but they are not persuasive.

In the remarks, the applicant has argued that:

- The features of the invention are neither taught nor suggested by the combination of Cmelik, in view of Cooke.
- Cmelik neither teaches nor suggests the limitation analyzing the first instructions en masse to determine information representing an information flow according to the first instructions, then using that information to generate target instructions as recited in claims 5, 34, 32, and 39.

Examiner's response:

- Applicant's arguments with respect to reference Cooke used to reject claims have been considered but are moot in view of new ground(s) of rejection.
- Cmelik does teach the limitations taught in claims 5, 34, 32, and 39. Cmelik disclose instructions are translated based on the occurrence of the conditions which existed at the beginning of a translation of a set of target instructions which is similar to analyzing the instruction then breaking them down as per instructions (see the rejection of this office action).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

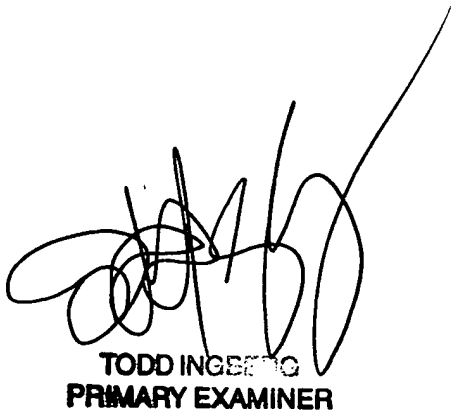
Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**.

The examiner can normally be reached on **8:30 am to 6:00 pm** Monday to Friday except every other Friday and federal holidays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Kakali Chaki** can be reached on **(571) 272-3719**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
Patent Examiner
Art Unit 2124
Jan 10, 2005



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